REMARKS

Reconsideration of this application is respectfully requested. Claims 1, 2, 7, 8, and 9 stand objected to because of informalities. Claim 11 stands rejected under 35 U.S.C. § 112 first paragraph. Claims 1-10 stand rejected under § 35 U.S.C. 102(e) as being anticipated by Guccione et al., U.S Patent number 6,216,259. The disclosure stands objected to because of informalities.

Claims 1-11 have been canceled. New claims 12-22 have been added.

The Office Action objected to the disclosure because "Applicant's request to cancel Figure 3c has been entered [and] Applicant must now delete all references to Figure 3c in the specification." Applicant submits a new Brief description of the drawings paragraph to delete the only reference to figure 3c. Applicant respectfully submits that the objection to the disclosure has been overcome.

The Office Action objected to claims 1, 2, 7, 8, and 9 because of informalities. The Office Action rejected claim 11 under 35 U.S.C. § 112 first paragraph. The Office Action rejected claims 1-10 under § 35 U.S.C. 102(e) as being anticipated by Guccione. Applicant canceled claims 1-11 rendering the above objections and rejections moot.

Applicant respectfully submits new claims 12-22 are patentable over Guccione.

Guccione discloses a configurable Programmable Logic Device, which receives program instructions on how to program its existing logic and connections. The programming instructions/bits are loaded into the programmable logic device to configure the device. Guccione discloses 1:

> 1. A method for configuration of a programmable logic device that is coupled to a processor using a library that comprises logic core generators and one or more router core generators, each of the logic and router core generators including code that is executable and

embodies design information, comprising the steps of:

executing a program on the processor, the program including instructions that reference selected ones of the logic core generators for functions to be provided by the programmable logic device;

generating by one or more of the logic core generators in response to the program, logic core definitions that define at least two logic cores;

generating by the router generators in response to the program, at least one router core definition that defines a coupling of the logic cores in the programmable logic device;

generating programming bits from the logic core definitions and router core definition in response to the program; and

loading the programmable logic device with the programming bits in response to the program.

(Col. 15, Lns. 1-10) (Emphasis Added)

Guccione warns that a user must take care when configuring a connection between two configurable blocks of logic (CLB) on the Programmable Logic Device because the existing connection or CLB may be already being used by another system resource. Guccione discloses:

> This router core object has a width of zero because it consumes no CLB logic. This core uses the direct connect signal lines between CLBs. Note that since the present method replaces a more elaborate automatic routing algorithm, it is left to the user to ensure that these routing resources are not in use.

(Col. 11, Lns 7-12) (Emphasis Added)

In contrast, new independent claim 12 states:

> 12. A computer core having an interface to communicate with other cores, wherein the interface contains a plurality of interface signal carriers that are configurable, at compilation, such that at least of one of the interface signal carriers is selectively physically present in the interface or not physically present, wherein not physically present means that a route connection is not generated for an interface signal carrier selected to be not physically present.

Guccione does not disclose an interface signal carriers that is configurable such that the interface signal carriers is selectively physical present in the interface or not physically present.

Given that new claims 13-15 depend from and include the limitations of claim 12, applicant submits that claims 13-15 are patentable over Guccione.

Similarly, applicant respectfully submits new claim 16 is patentable over Guccione. Guccione discloses that a core on the disclosed Programmable Logic Device is a block logic to provide an elementary level function such as adding, multiplying, on/off flip flops etc. Guccione discloses:

> The core library 206 is a collection of macrocell or "core" generators that are implemented as Java classes. The cores are generally parameterizable and relocatable within a device. Examples of cores include counters, adders, multipliers, constant adders, constant multipliers, flip-flops and other standard logic and computation functions. (Col. 4 Lns. 39-45)
>
> Selected functions provided by the core library 206 (FIG. 2) are invoked at step 304 to generate logic core definitions. The functions selected are those required to generate one or more logic cores for implementation on the programmable logic device. (Col. 5 Lns. 39-43)

New independent claim 16 states:

> 16. A core on a system on a chip having an interface, wherein the interface contains a plurality of interface signal carriers that are configurable, at compilation, such that at least of a first interface signal carriers is configurable to support different levels of functionality for the interface.

Guccione does not disclose core on a system on a chip that has an interface, which is configurable to support different levels of functionality for the interface.

Given that new claims 17 and 18 depend from and include the limitations of claim 16, applicant submits that claims 17 and 18 are patentable over Guccione.

Similarly, applicant respectfully submits new claim 19 is patentable over Guccione. New claim 19 discloses:

> 19. A method for generating at compilation a core interface for a system on a chip to enable re-use of the core with a different interface configuration, the method comprising:
> providing configurable source code representative of the core interface for the system on a chip and identifying parameters of the core interface;
> defining configuration parameters of the core interface; and
> generating the core interface for the system on a chip from the configurable source code representative of the core interface and the identified parameters of the core interface configurable in accordance with the defined configuration parameters of the core interface.

Guccione does not disclose a core interface for a core on a system on a chip to enable re-use of the core with a different interface configuration. Guccione does not disclose generating the core interface for the system on a chip from the configurable source code representative of the core interface and the identified parameters of the core interface configurable. Given that new claims 20-22 depend from and include the limitations of claim 19, applicant submits that claims 20-22 are patentable over Guccione.

Support for new claims 12-22 can be found throughout the specification. However, applicant specifically directs the examiner's attention to pages 2-5, and 8-10 as well as figures 1a-1c, 2a, 2b, and 4.

Conclusion

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. A petition for an extension of time is submitted with this amendment. Applicant reserves all rights with respect to the application of the doctrine equivalents. If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,
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